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(54) Semiconductor memory device with a refresh mechanism.

(57) A semiconductor memory device with a refresh mechanism having a plurality of memory cells (100) integrated on a semiconductor substrate, a plurality of word lines (W_L) and bit lines (Wd) each connected to the memory cells, a refresh control means (107) for successively selecting the word lines and refreshing the memory cells word line by word line in a refresh period and a timing means (102) connected to the word lines.

The timing means (102) is activated whenever the word line connected to it is selected during an access period and emits a 'refresh not required' signal and then causes the next refresh operation to be skipped for that word line.

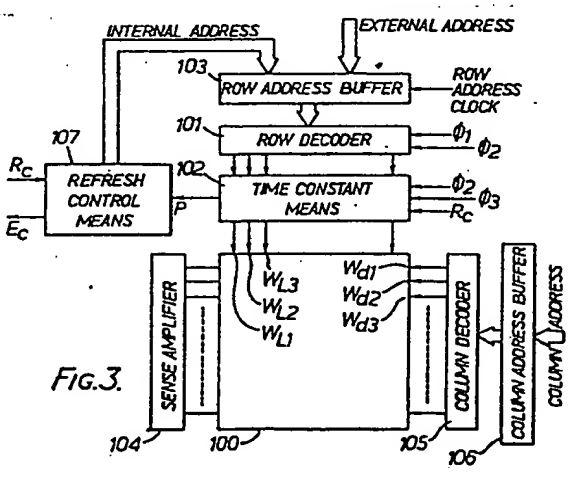

FIG.3.

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'Semiconductor Memory Device'

The present invention relates to a semiconductor memory device with a refresh mechanism such as a memory device consisting of dynamic memory cells, and more particularly to a semiconductor memory device with an improved refresh mechanism.

Various types of semiconductor memory with a rewrite facility have come into use of late, the commonest being the memory cell illustrated in Figure 1, consisting of one MOS transistor 1 and one MOS capacitor 2. In this memory cell, the gate of the MOS transistor 1 is connected to the word line, while the drain is connected to the digit line, and the data for storage is stored in the MOS capacitor 2 in the form of an electric charge. When a memory device, e.g. a dynamic random access memory (RAM), is formed from memory cells of this kind, these memory cells M are connected at the intersections of a plurality of word lines WL and a plurality of bit lines Wd arranged in matrix form, as shown in Figure 2.

In a dynamic RAM constructed in this way, data is stored as described above in the form of an electric charge, but some time after writing in the data the charge stored in the MOS capacitor 2 is lost because of leakage current, etc. If the data is left, after being written into the MOS capacitor 2, until a read-out is required, what has been stored in the MOS capacitor 2 may become corrupted. Also, the charge stored in the MOS capacitor 2 can be increased or decreased by soft errors. 'Soft errors' here means corruption of the data stored in the capacitor of the memory cell or faulty action of the sense amplifier, due to invasion of the diffusion layer of the memory cell or bit line by rays absorbed in minute amounts by the package and semi-conductor

substrate.

In the case of a dynamic RAM, therefore, provision has been made hitherto for a refresh period every 2 msec, during which access is not possible. During this period, the data stored in the MOS capacitor 2 is rewritten for all bits - it is, in short, refreshed. Usually a refresh control circuit is used when this refresh operation takes place, selecting each word line in succession and refreshing the memory cells word line by word line.

However, this kind of conventional memory device involved the following problem. Because the word line selected during the access period were also thereby refreshed, this practice of refreshing all the bits on all the word lines during the refresh period meant that word lines not yet requiring to be refreshed were refreshed twice in succession. These unnecessary refresh operations increased the consumption of electric current, and were also inconvenient in that they made it impossible to shorten the refresh period, during which data could not be accessed.

The present invention seeks to provide a semiconductor memory device whereby word lines selected during the access period and therefore not requiring to be refreshed are not selected during the refresh period, and whereby also the consumption of electric power during the refresh period is reduced and the refresh period itself can be shortened.

Accordingly the invention provides timing means, activated by the selection of a word line during the access period, and connected to each word line, and on the basis of the information emitted by the timing means, only those word lines requiring to be refreshed are selected during the refresh period.

In other words, according to the present

invention, a semiconductor memory device with a refresh mechanism, in which a plurality of memory cells each consisting of one transistor and one capacitor are integrated in matrix form on a semiconductor substrate, is characterised by timing circuits connected to a plurality of word lines connected individually to the above-mentioned memory cells, each of these time constant circuits, when activated by the selection during the access period of the associated word line, being arranged to emit a 'refresh not required' signal until a predetermined time has elapsed; a refresh control circuit also being provided to refresh the memory cells word line by word line, selecting these word lines in succession, but omitting those word lines connected to time constant which emit the 'refresh not required' signal, during the refresh period.

Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings in which:

Figure 1 is a circuit diagram showing the layout of a memory cell;

Figure 2 is a schematic diagram of the layout of a dynamic RAM using the above-mentioned memory cell;

Figure 3 is a block diagram showing in schematic form the layout of the main parts of an embodiment of the present invention;

Figure 4 is a circuit diagram of the refresh control means included in Figure 3;

Figure 5 is a flow-chart explaining the working of the embodiment shown in Figure 3;

Figure 6 is a circuit diagram showing the layout of a row decoder and a time constant means shown in Figure 3;

Figure 7 is a signal waveform chart explaining the working of the circuit shown in Figure 6;

Figure 8 is a block diagram showing in schematic form the layout of the main parts of another embodiment of the present invention; and

Figure 9 is a circuit diagram of the main parts of a refresh control means included in Figure 8.

Reference will now be made to the drawings, wherein like reference numerals designed identical or corresponding parts throughout the several views.

Figure 3 illustrates a block diagram of the present invention, in which reference numerals 100 designates an array of dynamic memory cells in which a plurality of memory cells M are integrated on a semiconductor substrate and are arranged in matrix form. Each cell consists of one MOS transistor and one MOS capacitor in the same manner as shown in Figure 1. Each of these memory cells M is connected at the intersection of a plurality of word lines WL and a plurality of digit lines Wd.

The word lines WL are connected to a row decoder 101 through a time constant means 102. The row decoder 101 is further connected to a row address buffer 103. A row address is supplied to the row address buffer 103 to select the word lines WL. The row address consists of two kinds of address i.e. an external address and an internal address, and one of these addresses is selectively supplied to the row address buffer 103 by a switching mechanism. A row address clock signal is supplied to the row address buffer 103, and the signals ϕ_1 and ϕ_2 are supplied to the row decoder 101. A signal ϕ_2 is also supplied to the time constant means 102 with signals ϕ_3 and Rc. The time constant means 102 emits a signal P which indicates that a refresh is not necessary in a refresh period.

A sense amplifier 104 and a column decoder 105 are connected to the digit lines Wd. A column buffer 106

to which a column address is supplied, is connected to the column decoder 105.

Reference numeral 107 designates a refresh control means which control the supply of the internal address which is used for a refresh of the memory cells in a refresh period. This control is carried out by detecting the signal P. Further, the refresh control means 107 is activated by receiving the signal Rc, and emits a signal Ec when the refresh period is completed.

Figure 4 shows a circuit diagram of the refresh control means 107. In this figure, reference numeral 10 designates a row address counter. The counter 10 is reset by the refresh clock Rc and incremented by 1 on receipt of a pulse from a pulse generator 11. As a result, the counter 10 supplies the internal address of, for example 8 bits, according to the count data. The internal address signal is also applied to a first circuit 12 consisting of a parallel circuit of a plurality of AND gates 13. This first circuit 12 detects when the data stored in the address counter 10 exceeds the highest available address, and emits the signal Ec. That is to say, when all bits of the internal address signal are ''1'', the first circuit 12 emits the signal ''1'', for example. This signal Ec shows that the refresh period is over, and the access period will be started.

The refresh control means also includes a second circuit 15. This second circuit 15 consists of an AND gate 16, inverter gate 17, a time delay circuit 18, AND gate 19 and OR gate 20. The pulse signal from the pulse generator 11 is supplied to the AND gates 16 and 19, and the signal P is supplied to AND gate 16 and NOT gate 17. As a result, when the signal P is ''1'', the pulses from the pulse generator 11 are supplied to the row address counter 10 through AND gate 16 and OR gate 20

in order to increment the data in the counter 10 by 1. When the signal P is ''0'', incrementation of the row address counter 10 is not carried out because AND gate 16 is closed. The delay time of the delay circuit 18 is so predetermined that the incrementation of the address counter 10 is stopped until refreshing of a word line is completed. Thus, when the signal P is ''0'', that is, when a refresh of its word line is necessary, the signal P is converted to ''1'' by inverter gate 17, and then delayed by the delay circuit 18. A signal which is delayed at a predetermined time is supplied to AND gate 19 as a signal RE which indicates the completion of the refresh process.

The time delay circuit 18, inverter gate 17, AND gate 19 and OR gate 20 can be eliminated if the signal RE is obtained by another method. For example, the signal RE can be obtained by the signals of a so-called row address clock chain.

The operation of the device constructed as described above is as follows referring to the flow-chart shown in Figure 5. First, when the refresh clock Rc is applied to the row address counter 10 -(a), the address counter 10 is reset -(b), and the address counter 10 is incremented by 1-(c). Next, the first circuit 12 checks whether or not the highest available address has been exceeded -(d). If it has been exceeded, the signal Ec, signalling that refresh period has been completed, is generated by the first circuit 12, and the access period is entered -(e). If the highest available address has not been exceeded, a test is performed to establish whether or not the word line corresponding to the address requires to be refreshed -(f). If the signal P is ''1'', that is, refreshing is not required, the sequence returns to (c), and the address counter 10 is once again incremented by 1. If the signal P is ''0'', that is

refreshing is required, the incrementation of the address counter 10 is stopped -(g), and the word line corresponding to the address is refreshed -(h). After completion of the refresh of this word line, the sequence returns to (c), i.e. the pulse from the pulse generator 11 is supplied to the address counter 10 through AND gate 19 and OR gate 20, the address counter 10 is incremented by 1, and the operation described above is repeated.

The time taken for the sequence (c)-(g) described above is shorter than the time taken to refresh one word line because the pulse generator 11 generates pulses at intervals shorter than the time taken to refresh one word line, and refreshing a word line previously accessed is thus skipped quickly. Thus the time taken to refresh a word line previously accessed in a conventional device is not substantially necessary in the present invention, and thus it is possible to shorten the refresh period.

Figure 6 is a circuit diagram showing the row decoder 101 and the time constant means 102 shown in Figure 3. The diagram depicts one word line only, as the layout is the same for all word lines. A MOS transistor 21, MOS transistors 22_0-22_7 connected in parallel and a MOS transistor 23 are connected in series to form a decoder. A source electrode of the transistor 21 is connected to a voltage source V_{DD} (for example, 5 volts), and the pulse signal ϕ_1 is supplied to a gate electrode of the transistor 21. Drain electrodes of the transistors 22_0-22_7 are connected to a voltage source V_{SS} (for example, 0 volts). The pulse ϕ_2 is supplied to a source electrode of the transistor 23. If the pulse signal ϕ_1 is high and address input signals A_{R0}-A_{R7} are low, the voltage potential of point R becomes high. This means that this word line is selected by the decoder 101. The output signal of the decoder is supplied to the

transistor 23.

The time constant means 102 consists of MOS tranistors 24-28 and a parallel circuit of a variable resistor 31 and a capacitor 32. The source electrode of the transistor 24 is connected to a drain electrode of the transistor 23, and the drain electrode of the transistor 24 is connected to the source electrode of the transistor 25. The gate electrode of the transistor 24 is connected to the connection point of the transistors 26 and 27. The drain electrode of the transistor 25 and the gate electrode of the transistor 27 are connected to a parallel circuit of a resistor 31 and a capacitor 32. The voltage V_{DD} is supplied to the source electrode of the transistor 26, a pulse signal $\emptyset_2$ is supplied to the gate electrode of the transistor 25 and a pulse signal $\emptyset_3$ is supplied to the gate electrode of the transistor 26. The transistors 27 and 28 are connected in series, and the refresh clock signal R_C is supplied to a gate electrode of the transistor 28. A word line W_L is connected to the interconnecting point of the transistors 24 and 25.

The operation of the circuit described above is as follows, referring to the timing chart shown in Figure 7. During an access cycle, firstly, the point R is precharged by the clock $\emptyset_1$. Then, address input signals A_R (A_{RO}-A_R) are supplied. If the address input signals A_R are low and clocks $\emptyset_2$ and $\emptyset_3$ are then supplied, transistors 23-26 turn on. As a result, the refreshing of the selected word line is started. Figure 7 shows that three word lines WL_1, WL_2, and WL_3 are selected for refreshing in the access cycle.

At the same time the word line is selected for refreshing, the capacitor 32 is also charged to the 'high' potential, and the capacitor 32 is discharged, via the resistor 31, when the clock $\emptyset_2$ goes low.

Consequently, the potential at point P gradually alters from 'high' to 'low'. The time constant of the discharge is determined by the product CR of the resistance R of the resistor 31 and the capacitance C of the capacitor 32, and can be set to suit requirements such as the maximum permitted refresh intervals, in order to select the resistance value.

Figure 7 shows the potentials P_{WL1}, P_{WL2} and P_{WL3}, corresponding to the word lines WL_1, WL_2 and WL_3 respectively.

During the refresh cycle, when the refresh clock R_C goes high, the transistor 28 switches on. If the potential P is still 'high', the transistor 27 is also on and the potential at point Q is taken low. Hence the transistor 24 will stay off even when the clocks $\emptyset_1$, $\emptyset_2$, and $\emptyset_3$ go high, and the word line stays low. The result is, therefore, that there is no refreshing of the word line corresponding to the address. In such a circumstance, the signal P (''1'') is supplied to the refresh control means 107, and the incrementation of the row address counter 10 is carried out.

If, however, a fixed time after the charging of the capacitor 32 has elapsed, the potential at point P becomes ''low'', the transistor 27 switches off and the potential at point Q is taken 'high' when the clock $\emptyset_3$ goes high. In such a circumstance, the row address counter 10 in the refresh control means 107 is not incremented, and the word line corresponding to the address is refreshed.

Figure 7 shows the case in which the word line W_{L3} is not refreshed because the potential P_{WL3} is still 'high'.

As described above, when the potential at point P is high during the refresh period, that is to say, in the event that the clocks $\emptyset_1$, $\emptyset_2$, and $\emptyset_3$ go high

when refreshing is not required in respect of that word line, a pulse emitted from the pulse generator 11 is supplied to the row address counter 10 to increment it by 1. By this means, a word line not requiring refreshing is not selected during the refresh period.

Thus in this embodiment, by setting at an appropriate value of CR time constant, refreshing of word line not selected during the refresh period because of previous access can be effected in the next refresh period before the data in the memory cells connected to those word lines becomes corrupted. The electric power consumption needed for one refresh operation can therefore be reduced, and the refresh period shortened.

Figure 8 shows another embodiment of the present invention. In this embodment the memory cells are divided into a plurality of blocks A-E, and the refresh is carried out from block to block. One block corresponds to fifty word lines, for example, and the time constant means 102_A-102_E, the configuration of which is the same as that shown in Figure 6 are respectively connected only to the first word lines WL_A-WL_E of each block. Conventional refresh circuits are connected to the remaining word lines. If the time constant means connected to the first word line WL_A of the block A emits the signal P indicating the refresh is not required, all word lines in the block A are unconditionally skipped. If the time constant means connected to the first word line of the block A detects that the refresh is necessary, all word lines in the block A are sequentially selected and refreshing is carried out word line by word line.

Figure 9 is a circuit diagram showing the main parts of a refresh control means 108 to establish the above-mentioned operation. The refresh control means 108 consists of a row address counter 10, a pulse generator

11, a counter 51, NOT gate 52, AND gates 53 and 55 and AND gate circuits 54 and 56. The counter 51 emits a pulse in every fifty pulses from the pulse generator 11, and supplies the output signal to AND gate 54. Assuming now that the signal P emitted from the time constant means connected to the first word line WL_A of block A is 'high', AND gate 53 opens, and then the row address counter 10 is incremented by the pulses from the pulse generator 11. When the row address counter 10 reaches a count of fifty, the counter 51 emits the output signal, and the output from the row address counter is then transferred to the row address buffer 103 through AND gate circuit 54. If the signal P is 'low' on the other hand, the signal P is converted to 'high' by NOT gate 52. The output signal of the NOT gate 52 is supplied to AND gates 55 and AND gate circuit 56. Therefore, the row address counter 10 is incremented by the pulses from the pulse generator 11, and each address corresponding to the address counter 10 is sequentially transferred to the row address buffer 103 through AND gate circuit 56.

As described above, according to the second embodiment of the present invention, the same effects as that described in the former embodiment can be obtained, when the dynamic memory is used especially for a data transfer apparatus or a static image treatment apparatus.

This invention is not restricted to the embodiments described above. For example, the time constant means referred to above need not be constituted by a resistor and a capacitor connected in parallel, but all that is necessary is that it should be activated by the selection of the word line in an access period, and that its output should alter in one direction or after a given period of time. Further, the refresh control means is not confined to the layout described above and illustrated by Figures 4 and 9, but may be varied as

appropriate.

CLAIMS

1. A semiconductor memory device comprising a plurality of memory cells (100) each consisting of one transistor (1) and one capacitor (2) a plurality of word lines (W_L) for addressing said memory cells, a plurality of digit lines (Wd) for reading and/or writing the data of said memory cells, an access control means (101, 103) for accessing said memory cells by selecting said word lines, a refresh control means (107) for successively selecting said word line connected to each of said memory cells and refreshing said memory cells word line by word line in a refresh period, characterised in that a timing means (102) is connected to each of said word lines, each of said timing means (102) being so arranged that it is activated whenever the word line connected to it is selected during an access period and being arranged to supply a 'refresh not required' signal until a predetermined time has elapsed, said refresh control means (107) being arranged to detect said 'refresh not required' signal and to then select the next word line.

2. A semiconductor memory device according to claim 1, wherein said refresh control means (107) includes;

a pulse generator (11),

a row address counter (10) for successively selecting said word lines in accordance with pulse signals from said pulse generator,

a first circuit means (12) for detecting the data in said row address counter and emitting a pulse signal indicating the end of said refresh period, and

a second circuit means (15) for incrementing said row address counter by 1 when said 'refresh not required' signal is supplied from said timing means and

stopping an incrementation of said row address counter when said 'refresh not required' signal is not supplied from said timing means.

3. A semiconductor memory device according to claim 1 or claim 2, wherein said timing means (102) includes;

a capacitor (32) arranged to be charged on selection of said word line,

a resistor (31) connected in parallel to said capacitor so as to discharge said capacitor with a time constant CR, where R is the resistance of said resistor and C is the capacitance of said capacitor.

4. A semiconductor memory device according to claim 3, wherein said time constant CR is variable.

5. A semiconductor memory device according to any preceding claim, wherein said transistor (1) is a MOS transistor whose gate is connected to said word line and whose drain is connected to said digit line.

6. A semiconductor memory device according to any preceding claim, wherein said capacitor (2) is a MOS capacitor which stores the data for storage in the form of an electric charge.

7. A semiconductor memory device according to any preceding claim, wherein said plurality of memory cells comprise a random access memory.

8. A semiconductor memory device according to any preceding claim in which said memory cells (100) are divided into a plurality of blocks (A-E), the first word lines (WL_A-WL_E) of each of the blocks being connected to

respective timing means (102) which are activated whenever said first word line connected to it is selected during an access period and emitting a 'refresh not required' signal until a predetermined time has elapsed, whereby said refresh control means (107) selects in said refresh period all of the word lines in the first block whose word line is connected to a timing means which does not emit said 'refresh not required' signal.

9. A semiconductor memory device according to claim 8, wherein said refresh control means (107) includes a circuit (10, 51, 54) for supplying row address signals corresponding to the first word line of each of said blocks when said time constant means emits said 'refresh not required' signal.

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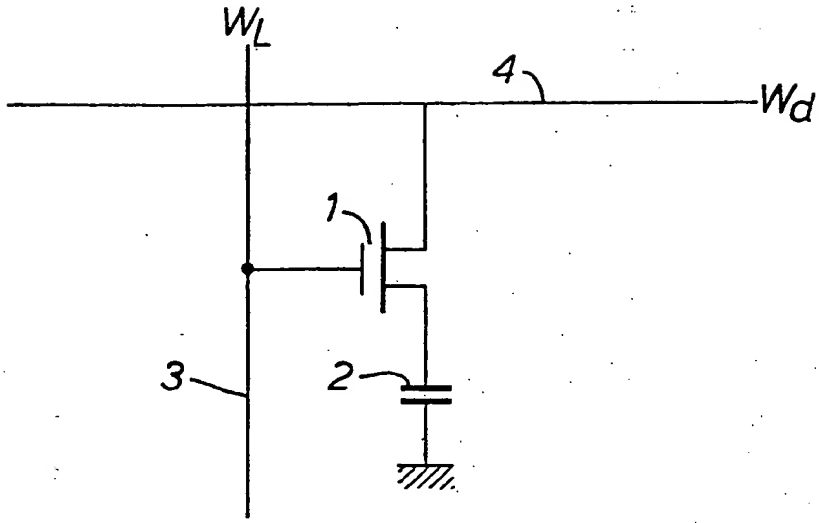

FIG. 1.

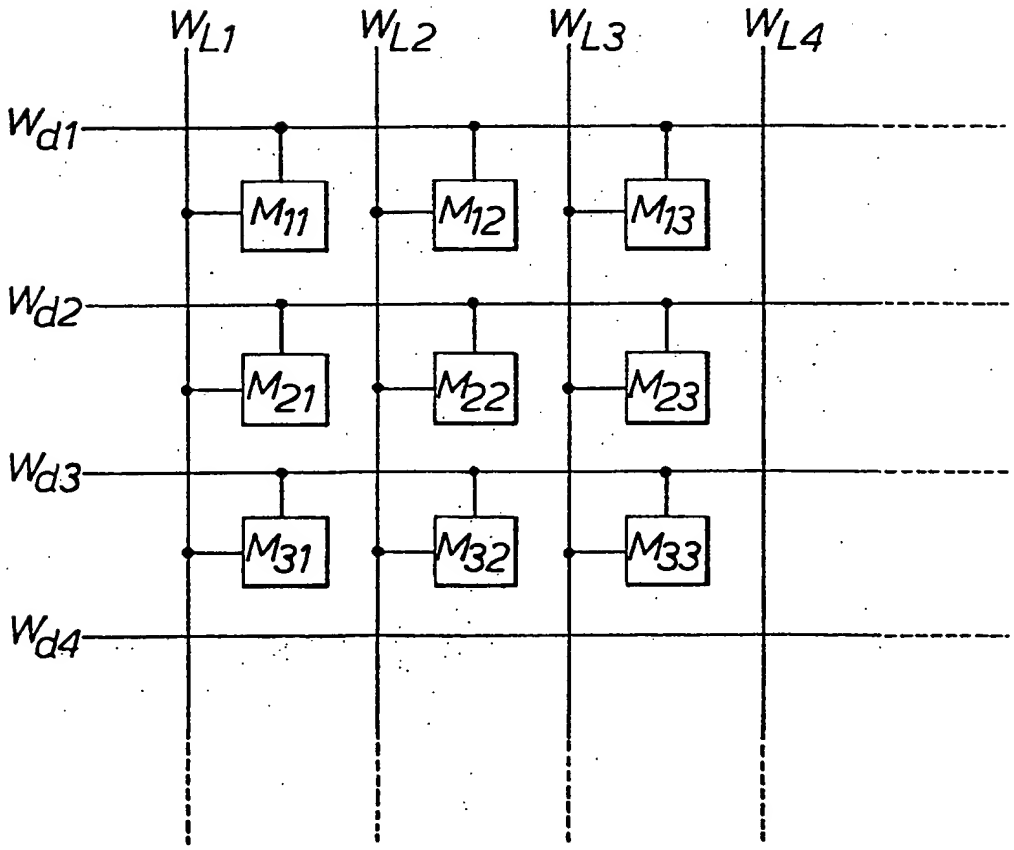

FIG. 2.

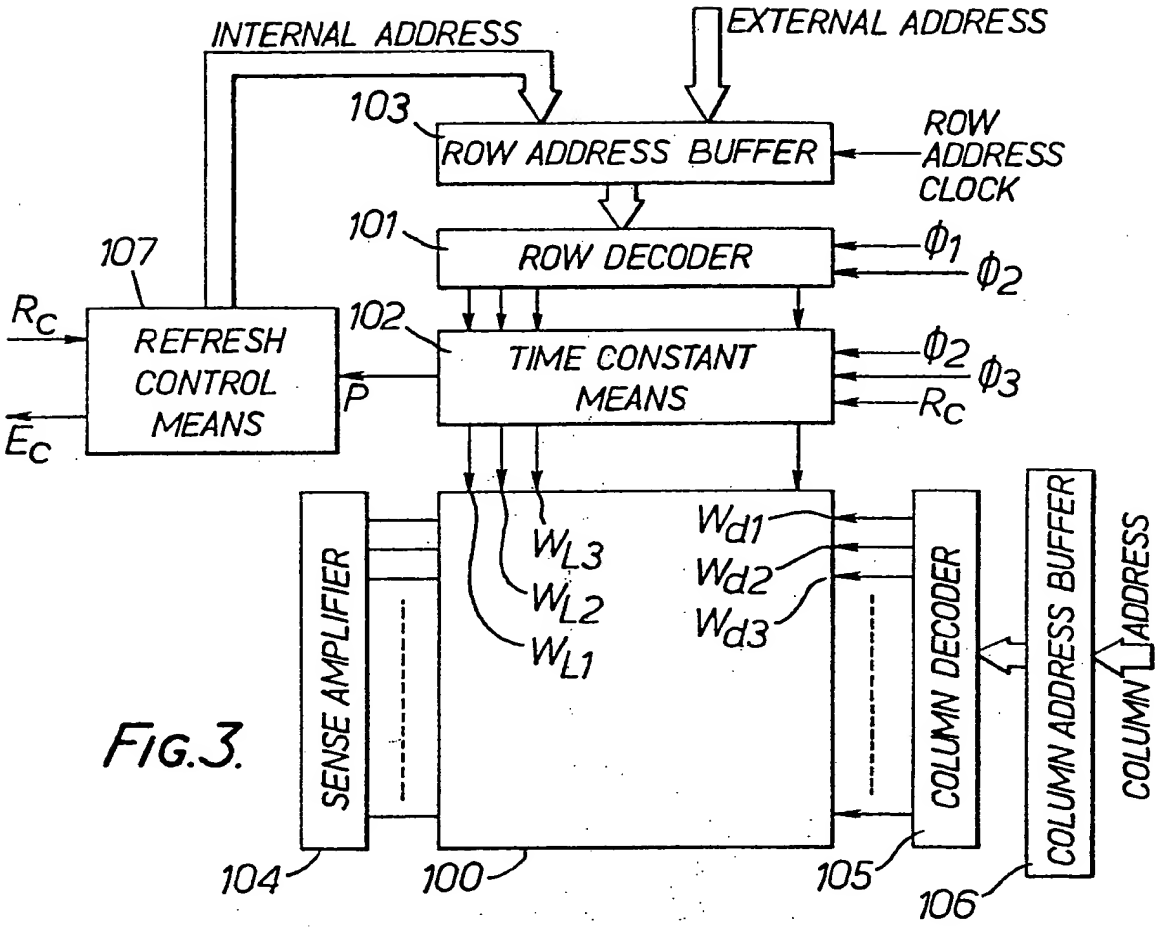

FIG.3.

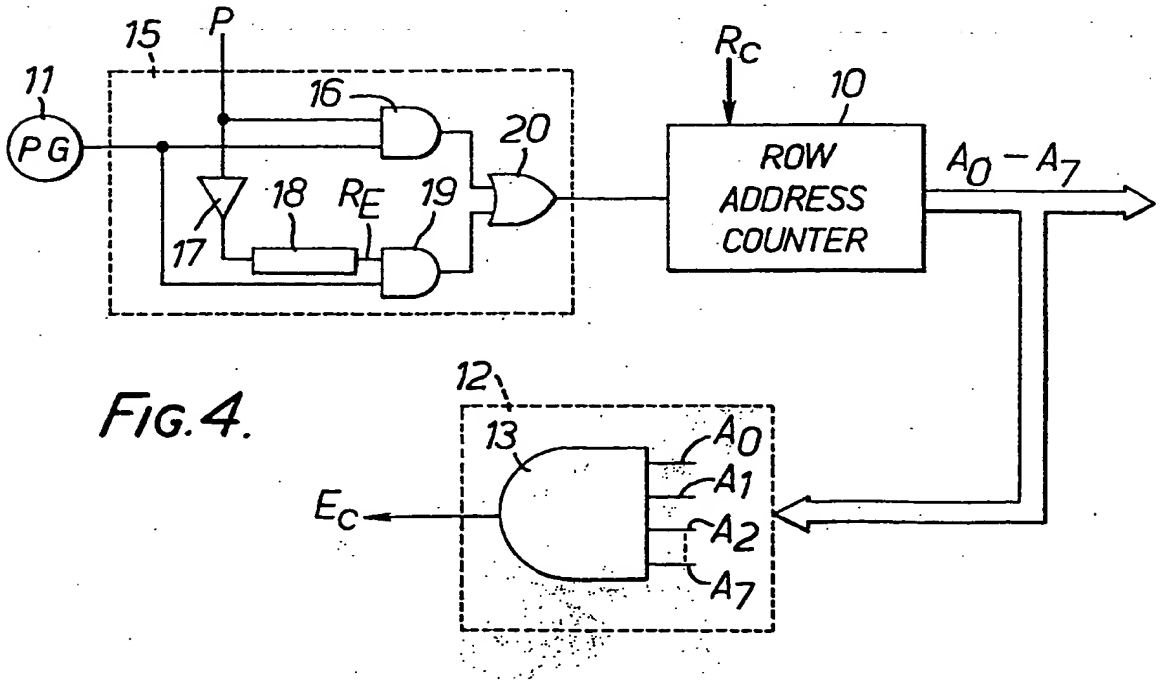

FIG.4.

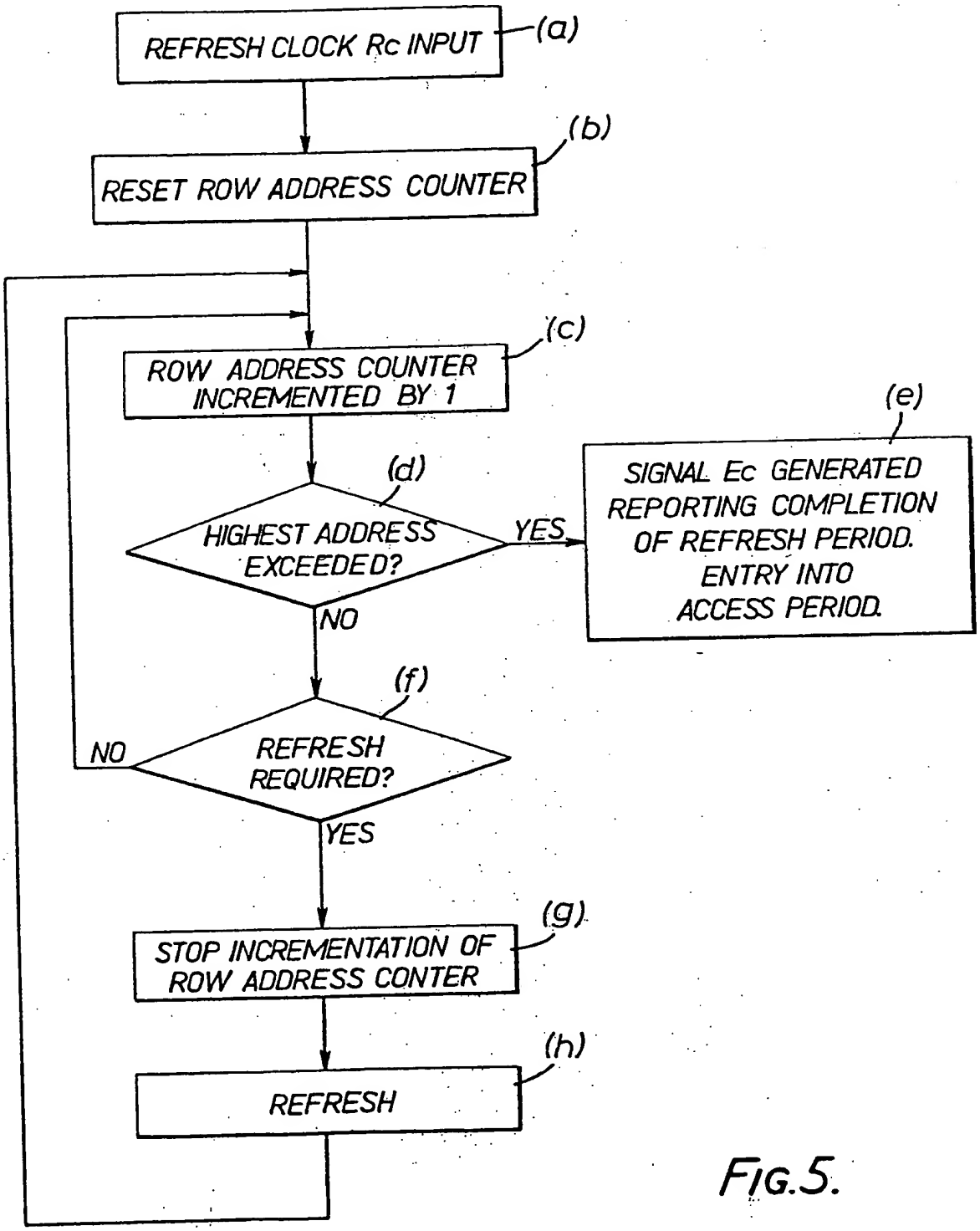

FIG.5.

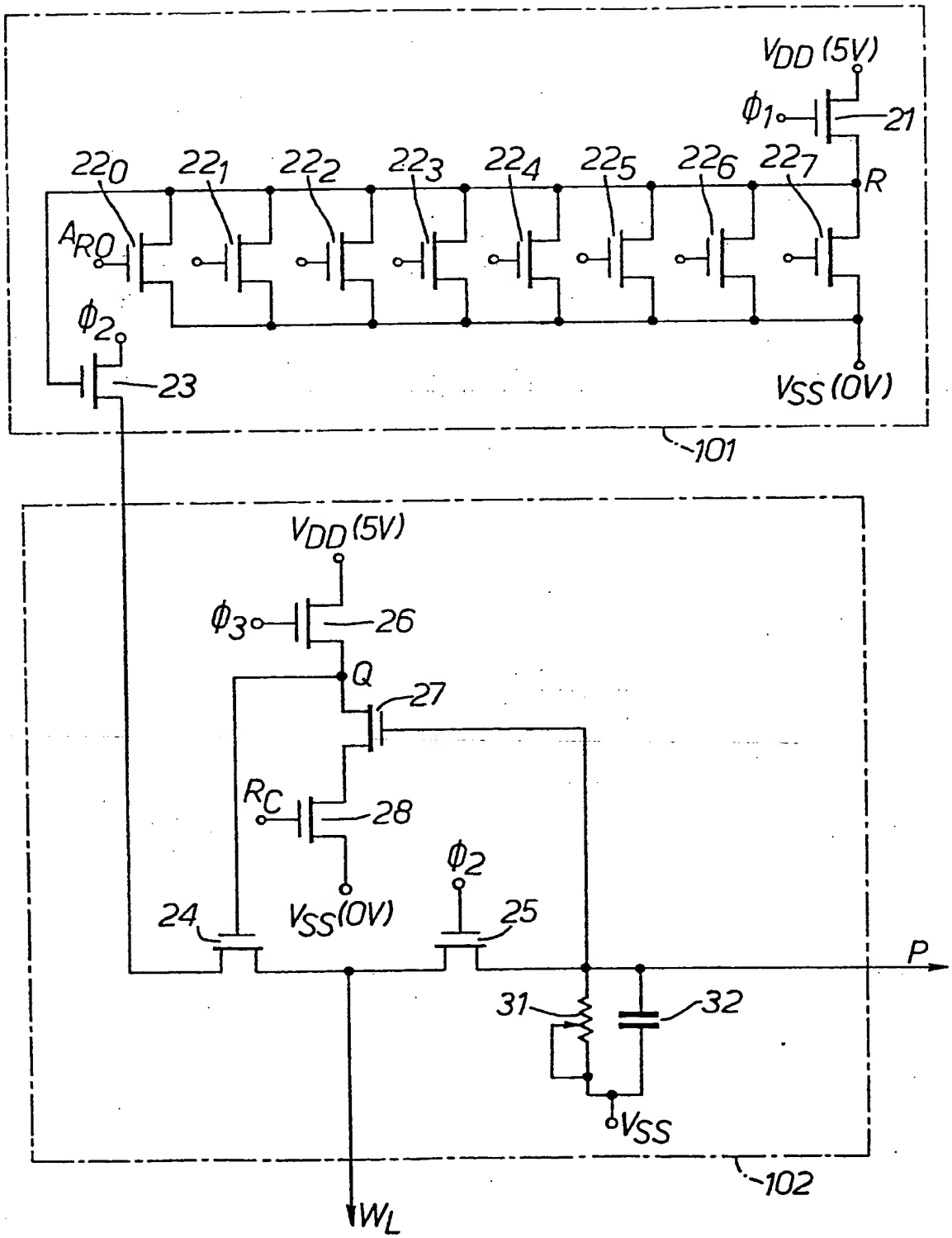

FIG. 6.

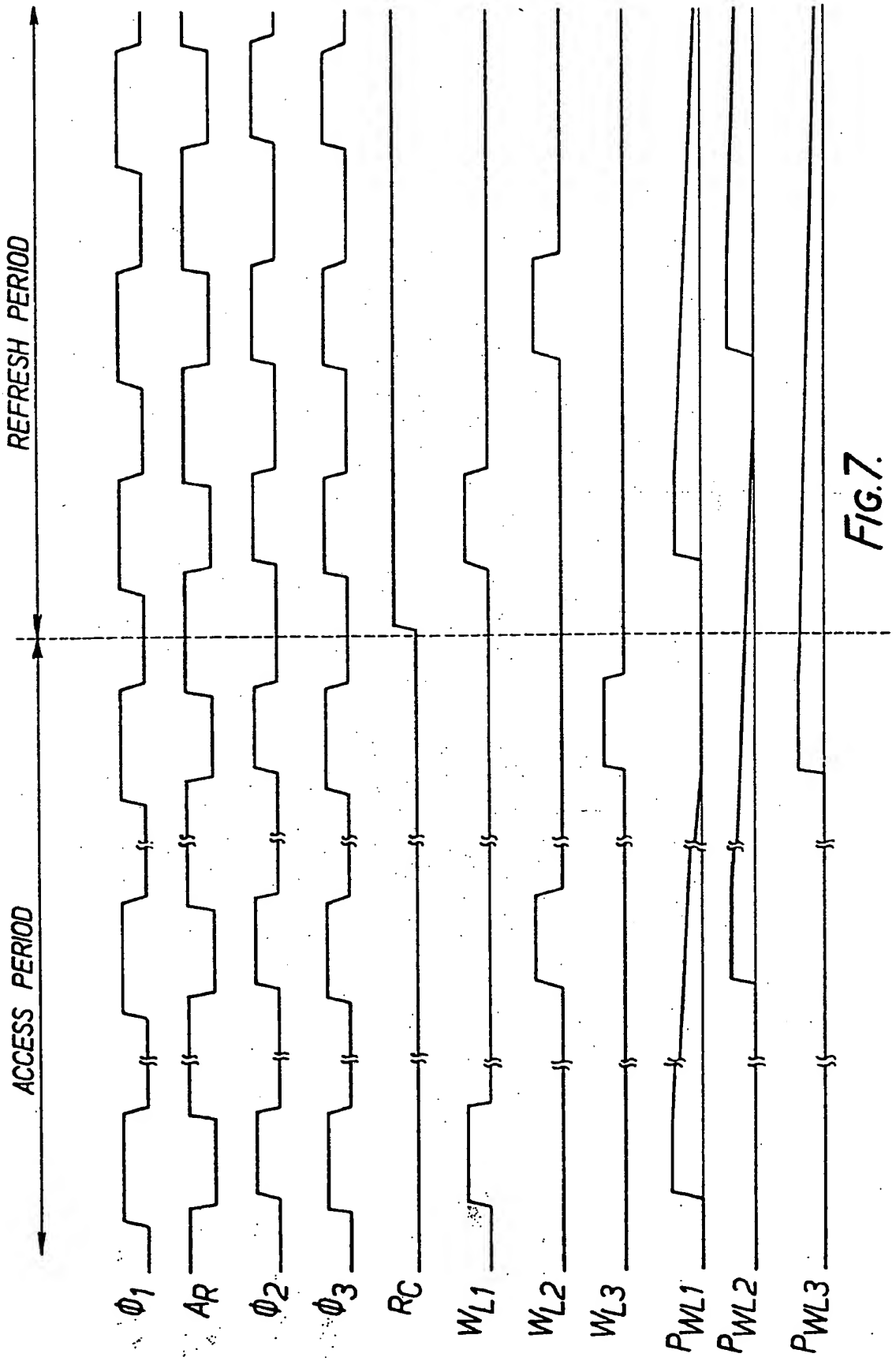

FIG.7.

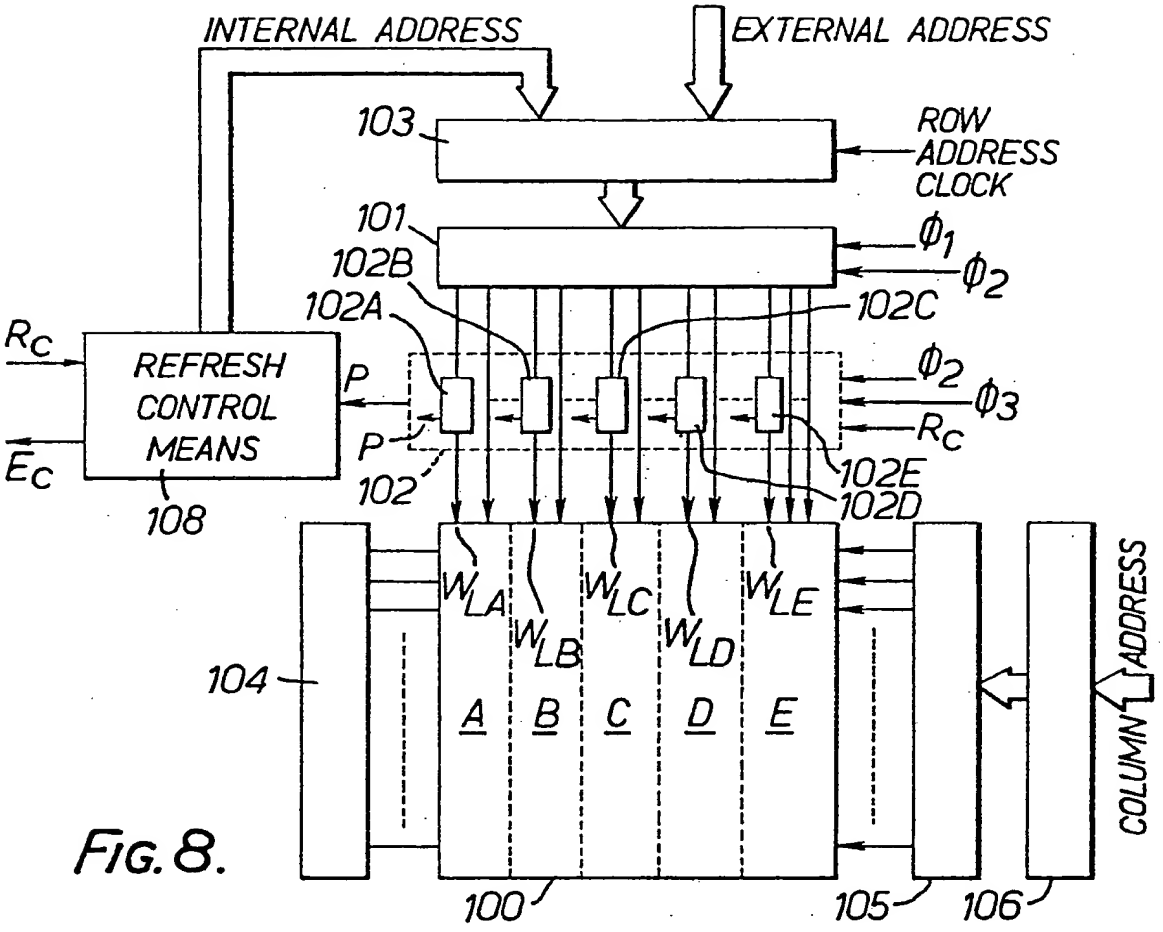

FIG. 8.

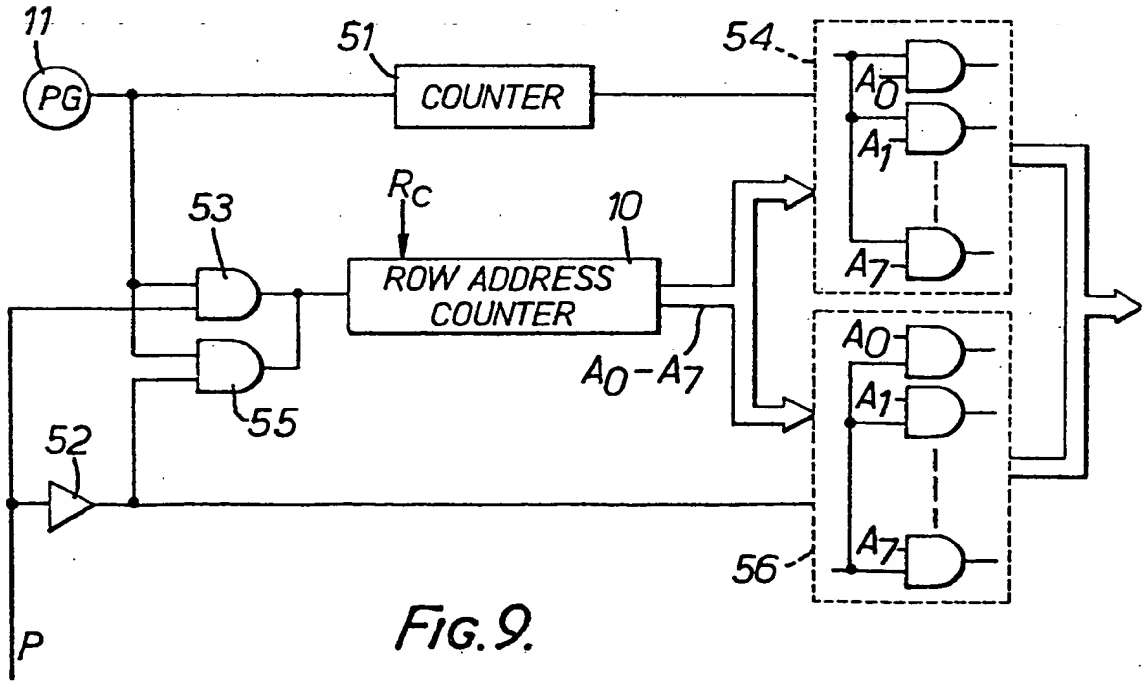

FIG. 9.

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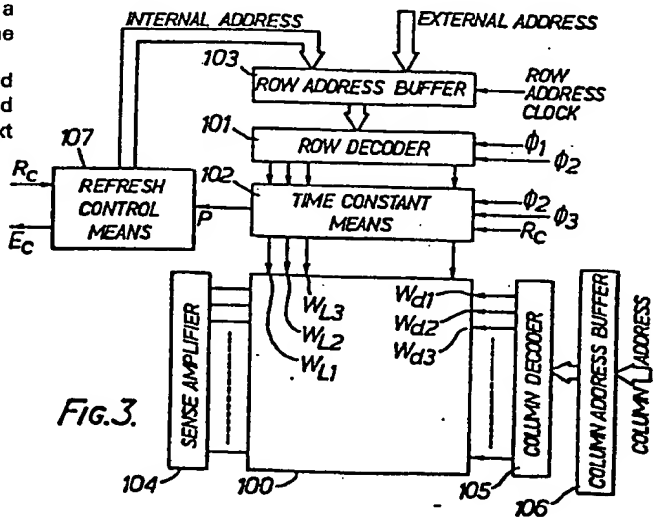

FIG.3.

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European Patent Office

EUROPEAN SEARCH REPORT

Application number 0116774

EP 83 30 7761

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
X	US-A-4 292 676 (HENIG) * Column 1, line 42 - column 2, line 52 *	1-2,5-7	G 11 C 11/24
A	US-A-3 858 184 (DE VRIES) * Claims *	1-2	
A	US-A-3 737 879 (GREENE) * Abstract *	1-2	
A	US-A-3 852 800 (OHWADA) * Column 1, line 53 - column 2, line 8 *	1-2, 5-7	

TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

G 11 C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23-06-1986	SGURA S.

CATEGORY OF CITED DOCUMENTS

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